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Capacitors, DRAM Arrays, Monolithic Integrated Circuits, And Methods Of Forming Capacitors, DRAM Arrays, And Monolithic Integrated Circuits

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TECHNICAL FIELD

The invention pertains to semiconductor capacitor constructions and to methods of forming semiconductor capacitor constructions. The invention is thought to have particular significance in application to methods of forming dynamic random access memory (DRAM) cell structures, to DRAM cell structures, and to integrated circuitry incorporating DRAM cell structures.

BACKGROUND OF THE INVENTION

A commonly used semiconductor memory device is a DRAM cell. A DRAM cell generally consists of a capacitor coupled through a transistor to a bitline. A semiconductor wafer fragment 10 is illustrated in Fig. 1 showing a prior art DRAM array 83. Wafer fragment 10 comprises a semiconductive material 12, field oxide regions 14, and wordlines 24 and 26. Wordlines 24 and 26 comprise a gate oxide layer 16, a polysilicon layer 18, a silicide layer 20 and a silicon oxide layer 22. Silicide layer 20 comprises a refractory metal silicide, such as tungsten silicide, and polysilicon layer 18 typically comprises polysilicon doped with a conductivity enhancing dopant. Nitride spacers 30 are laterally adjacent wordlines 24 and 26.

Electrical node locations 25, 27 and 29 are between wordlines 24 and 26 and are electrically connected by transistor gates comprised by wordlines 24 and 26. Node locations 25, 27 and 29 are diffusion regions formed within semiconductive material 12.

A borophosphosilicate glass (BPSG) layer 34 is over semiconductive material 12 and wordlines 24 and 26. An oxide layer 32 is provided

between BPSG layer 34 and material 12. Oxide layer 32 inhibits diffusion of phosphorus from BPSG layer 34 into underlying materials.

Conductive pedestals 54, 55 and 56 extend through BPSG layer 34 to node locations 25, 27 and 29, respectively. Capacitor constructions 62 and 64 contact upper surfaces of pedestals 54 and 56, respectively. Capacitor constructions 62 and 64 comprise a storage node layer 66, a dielectric layer 68, and a cell plate layer 70. Dielectric layer 68 comprises an electrically insulative layer, such as silicon nitride. Cell plate layer 70 comprises conductively doped polysilicon, and may alternatively be referred to as a cell layer 70. Storage node layer 66 comprises conductively doped hemispherical grain (HSG) polysilicon.

A conductive bitline plug 75 contacts an upper surface of pedestal 55. Bitline plug 75 may comprise, for example, tungsten. Together, bitline plug 75 and pedestal 55 comprise a bitline contact 77.

A bitline 76 extends over capacitors 62 and 64 and in electrical connection with bitline contact 77. Bitline 76 may comprise, for example, aluminum.

The capacitors 62 and 64 are electrically connected to bitline contact 77 through transistor gates comprised by wordlines 26. A first DRAM cell 79 comprises capacitor 62 electrically connected to bitline 76 through a wordline 26 and bitline contact 77. A second DRAM cell 81 comprises capacitor 64 electrically connected to bitline 76 through wordline a 26 and bitline contact 77. DRAM array 83 comprises first and second DRAM cells 79 and 81.

If capacitors 62 and 64 are inadvertently shorted together, a so-called "double bit failure" will occur. Such double bit failures can occur if a stray piece of polysilicon, or HSG polysilicon, breaks off during formation of DRAM array 83 and disadvantageously electrically connects capacitors 62 and 64. Prior art capacitor fabrication methods employ chemical-mechanical polishing (CMP) of HSG polysilicon. HSG polysilicon pieces can break off during such CMP processes and cause double bit failures. It would be desirable to develop alternative DRAM constructions which could be formed by methods avoiding double bit failures.

SUMMARY OF THE INVENTION

The invention includes a number of methods and structures pertaining to semiconductor circuit technology, including: methods of forming DRAM memory cell constructions; methods of forming capacitor constructions; DRAM memory cell constructions; capacitor constructions; and integrated circuitry. For instance, the invention encompasses a method of forming a capacitor wherein a mass of silicon material is formed over a node location, and wherein the mass comprises exposed doped silicon and exposed undoped silicon. The method can further include substantially selectively forming rugged polysilicon from the exposed undoped silicon and not from the exposed doped silicon. Also, the method can include forming a capacitor dielectric layer and a complementary capacitor plate proximate the rugged polysilicon and doped silicon.

As another example, the invention encompasses a capacitor having a capacitor dielectric layer intermediate a first capacitor plate and a second capacitor plate, wherein at least one of the first and second capacitor plates has a surface against the capacitor dielectric layer, and wherein said surface comprises both doped rugged polysilicon and doped non-rugged polysilicon.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a schematic cross-sectional view of a semiconductor wafer fragment comprising a prior art DRAM array.

Fig. 2 is a schematic cross-sectional process view of a semiconductor wafer fragment at preliminary processing step of a processing method of the present invention.

Fig. 3 is a view of the Fig. 2 wafer fragment at a processing step subsequent to that of Fig. 2.

Fig. 4 is a view of the Fig. 2 wafer fragment at a processing step subsequent to that of Fig. 3.

Fig. 5 is a view of the Fig. 2 wafer fragment at a processing step subsequent to that of Fig. 4.

Fig. 6 is a view of the Fig. 2 wafer fragment at a processing step subsequent to that of Fig. 5.

Fig. 7 is a view of the Fig. 2 wafer fragment at a processing step subsequent to that of Fig. 6.

Fig. 8 is a view of the Fig. 2 wafer fragment at a processing step subsequent to that of Fig. 7.

Fig. 9 is a top view of the Fig. 8 wafer fragment.

Fig. 10 is a view of the Fig. 2 wafer fragment at a processing step subsequent to that of Fig. 8.

Fig. 11 is a view of the Fig. 2 wafer fragment at a processing step subsequent to that of Fig. 10.

Fig. 12 is a view of the Fig. 2 wafer fragment at a processing step subsequent to that of Fig. 11.

Fig. 13 is a view of the Fig. 2 wafer fragment at a processing step subsequent to that of Fig. 12.

Fig. 14 is a view of the Fig. 2 wafer fragment at a processing step subsequent to that of Fig. 6 processed according to a second embodiment of the present invention.

Fig. 15 is a view of the Fig. 2 wafer fragment at a step subsequent to that of Fig. 14.

Fig. 16 is a top view of the Fig. 15 wafer fragment.

Fig. 17 is a view of the Fig. 2 wafer fragment at a step subsequent to that of Fig. 15.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Methods of forming DRAM arrays of the present invention are described with reference to Figs. 2-17, with Figs. 2-13 pertaining to a first embodiment of the invention, and Figs. 14-17 pertaining to a second embodiment of the invention. In describing the first embodiment of the present invention, like numerals from the preceding discussion of the prior art are utilized where appropriate, with differences being indicated by the suffix "a" or with different numerals.

Referring to Fig. 2, a semiconductor wafer fragment 10a is illustrated at a preliminary step of a process of the present invention. Wafer fragment 10a comprises a semiconductive material 12a, field oxide regions 14a, and a thin gate oxide layer 16a. Over gate oxide layer 16a is formed polysilicon layer 18a, silicide layer 20a and silicon oxide layer 22a. Silicide layer 20a comprises a refractory metal silicide, such as tungsten silicide, and polysilicon layer 18a typically comprises polysilicon doped with a conductivity enhancing dopant. Layers 16a, 18a, 20a and 22a can be formed by conventional methods.

Referring next to Fig. 3, polysilicon layer 18a, silicide layer 20a and silicon oxide layer 22a are etched to form wordlines 24a and 26a. Such etching can be accomplished by conventional methods. Between wordlines 24a and 26a are defined electrical node locations 25a, 27a and 29a, with

wordlines 26a comprising transistor gates which electrically connect node locations 25a, 27a, and 29a. Node locations 25a, 27a and 29a are diffusion regions formed within semiconductive material 12a.

Referring to Figs. 4 and 5, a nitride layer 28a is provided over wordlines 24a and 26a and subsequently etched to form nitride spacers 30a laterally adjacent wordlines 24a and 26a.

Referring to Fig. 6, an insulative material layer 34a is formed over material 12a and over wordlines 24a and 26a. Insulative layer 34a may comprise, for example, BPSG, and can be formed by conventional methods. Insulative layer 34a comprises an upper surface 35a. Openings 38a, 39a and 40a are formed extending through insulative layer 34a to node locations 25a, 27a and 29a, respectively.

Referring to Fig. 7, an undoped silicon layer 100 is formed over insulative layer 34a and within openings 38a, 39a and 40a. Undoped silicon layer 100 narrows openings 38a, 39a and 40a, but does not fill such openings. Undoped silicon layer 100 preferably has a thickness of from about 50 Angstroms to about 1000 Angstroms, with a thickness of about 300 Angstroms being most preferred. Undoped silicon layer 100 preferably comprises substantially amorphous silicon. Such substantially amorphous layer can be 5-10% crystalline. Undoped silicon layer 100 can be formed by conventional methods, such as, for example, by deposition utilizing either silane or disilane. For purposes of the continuing discussion, and for interpreting the claims that follow, "undoped" silicon is defined as silicon having a dopant concentration of less than 5×10^{18} atoms/cm^3, and "doped"

silicon is defined as silicon having a dopant concentration of at least 5×10^{18} atoms/cm^3. "Undoped" silicon preferably comprises less than or equal to 1×10^{18} atoms/cm^3, and "doped" silicon preferably comprises at least 1×10^{19} atoms/cm^3.

A doped silicon layer 102 is formed over undoped silicon layer 100 and within openings 38a, 39a and 40a. In the shown embodiment of the invention, doped layer 102 completely fills openings 38a, 39a and 40a. However, in alternative embodiments of the invention, such as the embodiment discussed below with reference to Figs. 14-17, layer 102 can only partially fill openings 38a, 39a and 40a. As will be appreciated by persons of ordinary skill in the art, the thickness of layer 102 will vary depending on whether layer 102 is chosen to completely fill openings 38a, 39a and 40a, or to partially fill such openings. Doped silicon layer 102 preferably comprises doped polysilicon, and can be formed by conventional methods.

After formation of layers 100 and 102, an upper surface of wafer fragment 10a is planarized to remove layers 100 and 102 from over insulative layer 34a. Such planarization can be accomplished by, for example, chemical-mechanical polishing (CMP).

Referring to Fig. 8, after the above-discussed planarization, pedestals 104, 106 and 108 remain in openings 38a, 39a and 40a (shown in Fig. 7), respectively. Pedestals 104, 106 and 108 comprise undoped silicon layer 100 and doped silicon layer 102, and are over node locations 25a, 27a and 29a, respectively. Pedestals 104, 106 and 108 also comprise exposed upper surfaces 116, 118 and 120, respectively.

Fig. 9 illustrates a top view of the Fig. 8 wafer fragment, and shows that pedestals 104, 106 and 108 actually comprise a core of doped silicon layer 102 surrounded by undoped silicon layer 100.

Referring again to Fig. 8, insulative layer 34a is selectively removed relative to the silicon of pedestals 104, 106 and 108 to form a new upper surface 37a lower than previous upper surface 35a (shown in Fig. 7). The preferred BPSG insulative layer 34a can be selectively removed relative to pedestals 104, 106 and 108 using a conventional oxide etch. The selective removal of insulative layer 34a exposes a sidewall surface 110 of pedestal 104, a sidewall surface 112 of pedestal 106, and a sidewall surface 114 of pedestal 108. Sidewall surfaces 110, 112 and 114 comprise undoped silicon layer 100. Additionally, in the shown embodiment a portion of undoped silicon layer 100 is below upper surface 37a of BPSG layer 34a, and remains unexposed. The depth of removal of insulative layer 34a can be controlled by a number of methods. For example, layer 34a could be removed via a timed etch. As another example, an etch stop layer could be formed within layer 34a at a desired depth of surface 37a. An example of a layer 34a comprising an etch stop layer is a layer comprising BPSG and having a silicon nitride etch stop layer formed within the BPSG at a level of upper surface 37a.

As exposed sidewall surfaces 110, 112 and 114 of pedestals 104, 106 and 108 comprise undoped silicon layer 100, and as exposed upper surfaces 116, 118 and 120 of the pedestals comprise exposed doped silicon layer 102, as well as exposed undoped silicon layer 100, the pedestals comprise exposed

doped silicon and exposed undoped silicon at the processing step of Fig. 8.

Referring to Fig. 10, a rugged polysilicon layer 122 is substantially selectively formed from the exposed undoped silicon of surfaces 110, 112 114, 116, 118, and 120 (shown in Fig. 8), and not from the exposed doped silicon of surfaces 116, 118 and 120. Rugged polysilicon layer 122 comprises materials selected from the group consisting of HSG and cylindrical grain polysilicon. The substantially selective formation of a preferred HSG polysilicon layer 122 from undoped silicon surfaces but not from doped silicon surfaces can be accomplished by the following process.

First, wafer fragment 10a is loaded into a conventional chemical vapor deposition (CVD) furnace and is subjected to an *in situ* hydrofluoric acid (HF) clean to remove native oxide. The *in situ* HF clean preferably comprises a flow rate of 85 standard cubic centimeters per minute (sccm) of HF gas and 8500 sccm of H_2O gas, at a pressure of 15 Torr, for a time of about 20 seconds. Wafer fragment 10a is then exposed to silane to form amorphous silicon seeds on the undoped silicon. Wafer fragment 10a is then annealed for approximately 20 minutes at about 560°C. The seeding and anneal steps convert undoped amorphous silicon into rugged polysilicon (such as hemispherical grain polysilicon), while leaving exposed doped silicon layers not converted to rugged polysilicon. It is noted that the above-described process for forming HSG polysilicon does not require disilane, and hence is different than the "pure" selective hemispherical grain deposition utilized in high vacuum tools with disilane.

After the formation of rugged polysilicon layer 122, a short polysilicon etch is performed to remove any monolayers of silicon deposited on insulative layer 34a during the above-described seeding step. Such polysilicon etch can be accomplished with conventional conditions, and may comprise either a wet etch or a dry etch.

The above-described process for forming rugged polysilicon layer 122 advantageously avoids formation of polysilicon on a back side (not shown) of wafer fragment 10a. The method can also avoid double bit failures by removing monolayers of silicon after formation of HSG.

Subsequent thermal processing of pedestals 104, 106 and 108 can out-diffuse dopant from doped polysilicon layer 102 into undoped silicon layer 100 (shown in Fig. 8), to convert unexposed portions of undoped silicon layer 100 into a doped polysilicon layer 119. Subsequent thermal processing can also out-diffuse dopant from doped polysilicon layer 102 into rugged polysilicon layer 122. Thermal processing to out-diffuse dopant from doped polysilicon layer 102 into adjacent undoped layers will typically comprise temperatures of 800° C or greater.

Referring to Fig. 11, a dielectric layer 124 is provided over insulative layer 34a and over pedestals 104, 106 and 108. Dielectric layer 124 will typically comprise silicon nitride and/or silicon oxide, although other suitable materials are known to persons of skill in the art. A capacitor cell plate layer 126 is provided over dielectric layer 124. Capacitor cell plate layer 126 will typically comprise doped polysilicon, but other suitable materials are known to persons of skill in the art.

Referring to Fig. 12, a patterned masking layer 128 is formed over pedestals 104 and 108, leaving pedestal 106 exposed. Subsequently, wafer fragment 10a is subjected to etching conditions which remove cell plate layer 126 and dielectric layer 124 from proximate pedestal 106. After such etching, pedestal 106 is electrically isolated from pedestals 104 and 108, with the only remaining electrical connection between pedestal 106 and pedestals 104 and 108 being through wordlines 26a. Methods for removing cell plate layer 126 and dielectric layer 124 from proximate pedestal 106 are known to persons of ordinary skill in the art.

Referring to Fig. 13, masking layer 128 is removed and an insulative layer 130 is formed over pedestals 104, 106 and 108, and over insulative layer 34a. Insulative layer 130 may comprise, for example, BPSG, and can be formed by conventional methods. A conductive bitline plug 75a is formed extending through insulative layer 130 and in electrical contact with pedestal 106. Pedestal 106 comprises rugged lateral surfaces 136 and an upper surface 118 which has a predominant portion not comprising rugged-polysilicon. As shown, the non-rugged polysilicon of upper surface advantageously provides a smooth landing region for bitline plug 75a.

Pedestal 106 and bitline plug 75a together form a bitline contact 77a. A bitline 76a is formed over bitline plug 75a and in an electrical connection with pedestal 106 through bitline plug 75a. Bitline 76a and bitline plug 75a may be formed by conventional methods.

The above-describe method can be used to avoid chemical-mechanical polishing of a rugged polysilicon layer, thus avoiding a potential source of double bit failures.

Fig. 13 illustrates a DRAM array 83a of the present invention. DRAM array 83a comprises capacitors 62a and 64a. Capacitors 62a and 64a comprise capacitor storage nodes 132 and 134, respectively, which comprise doped polysilicon layer 102, doped polysilicon layer 119 and rugged-polysilicon layer 122. As the doped polysilicon layer 119 is formed from the undoped silicon layer 100 (shown in Fig. 8), the undoped silicon layer 100 and doped silicon layer 102 of pedestals 104 and 108 in Fig. 8 together define capacitor storage nodes 132 and 134. Storage nodes 132 and 134 have rugged-polysilicon-comprising lateral surfaces 138 and 140, respectively. Storage nodes 132 and 134 further comprise top surfaces 116 and 120, respectively, which have predominant portions which do not comprise rugged-polysilicon.

Cell plate layer 126 and dielectric layer 124 are operatively proximate to storage nodes 132 and 134 so that the storage nodes, together with cell plate layer 126 and dielectric layer 124, form operative capacitors 62a and 64a. Dielectric layer 124 contacts rugged surfaces 138 and 140, as well as top surfaces 116 and 120 of storage nodes 132 and 134.

Capacitors 62a and 64a are connected to pedestal 106 through wordlines 26a. Capacitor 62a, together with bitline contact 77a and an interconnecting wordline 26a, comprises a first DRAM cell 79a. Capacitor 64a, together with bitline contact 77a and an interconnecting wordline 26a, comprises a second DRAM cell 81a.

A second embodiment of the invention is described with reference to Figs. 14-17. In describing the embodiment of Figs. 14-17, numbering similar to that utilized above for describing the embodiment of Figs. 2-13 is utilized, with differences being indicated by the suffix "b", or by different numbers.

Referring to Fig. 14, a wafer fragment 10b is shown at a processing step subsequent to that of the above-discussed Fig. 6. Wafer fragment 10b comprises wordlines 24b and 26b having constructions identical to that discussed above with regard to the prior art. Wafer fragment 10b further comprises node locations 25b, 27b and 29b between wordlines 24b and 26b. Wafer fragment 10b also comprises a semiconductor substrate 12b and field oxide regions 14b formed over substrate 12b.

An insulative material layer 34b is formed over wordlines 24b and 26b, and over semiconductive material 12b. Insulative layer 34b may comprise a number of materials known to persons of ordinary skill in the art, including BPSG. Openings 38b, 39b and 40b extend through insulative layer 34b to node locations 25b, 27b and 29b, respectively.

A first undoped silicon layer 146 extends over insulative layer 34b and within openings 38b, 39b and 40b. Undoped silicon layer 146 preferably comprises amorphous silicon, and preferably has a thickness of from about 50 Angstroms to about 500 Angstroms. Undoped silicon layer 146 can be formed by conventional methods, such as CVD. Undoped silicon layer 146 narrows openings 38b, 39b and 40b.

A doped silicon layer 148 is formed over undoped silicon layer 146 and within narrowed openings 38b, 39b and 40b. Doped silicon layer 148 preferably comprises polysilicon, and can be formed by conventional methods, such as CVD. Doped silicon layer 148 preferably has a thickness of from about 50 Angstroms to about 500 Angstroms, and preferably does not fill openings 38b, 39b and 40b. Rather, doped silicon layer 148 preferably further narrows openings 38b, 39b and 40b beyond where openings 38b, 39b and 40b were narrowed by undoped silicon layer 146.

A second undoped silicon layer 150 is formed over doped silicon layer 148 and within openings 38b, 39b and 40b. Undoped silicon layer 150 preferably comprises the same preferable materials of first undoped silicon layer 146. Accordingly, second undoped silicon layer 150 preferably comprises substantially amorphous silicon. Second undoped silicon layer 150 preferably has a thickness of from 50 to 500 Angstroms, and in the shown preferred embodiment does not fill openings 38b, 39b and 40b.

After formation of layers 146, 148 and 150, wafer fragment 10b is planarized to remove layers 146, 148 and 150 from over insulative layer 34b. Such planarizing may be accomplished by, for example, chemical-mechanical polishing. After the planarization of wafer fragment 10b, pedestals 104b, 106b and 108b (shown in Fig. 15) having upper surfaces 116b, 118b and 120b (shown in Fig. 15), respectively, remain within openings 38b, 39b and 40b.

Referring to Fig. 15, the material of insulative layer 34b is selectively removed relative to the silicon of pedestals 104b, 106b and 108b to form an

upper surface 37b of insulative layer 34b which is below upper surfaces 116b, 118b and 120b of pedestals 104b, 106b and 108b. The removal of insulative layer 34b exposes sidewalls 110b, 112b and 114b of pedestals 104b, 106b and 108b, respectively. The exposed sidewalls 110b, 112b and 114b comprise first undoped silicon layer 146. Additionally, in the shown embodiment a portion of undoped silicon layer 146 is below upper surface 37b of BPSG layer 34b, and remains unexposed. In the shown preferred embodiment, pedestals 104b, 106b and 108b comprise hollow interiors corresponding to openings 38b, 39b and 40b (shown in Fig. 14). The depth of removal of insulative layer 34b can be controlled by methods such as those discussed above with reference to Fig. 8 for controlling the depth of removal of insulative layer 34a.

Referring to Fig. 16, which is a top view of the Fig. 15 wafer fragment, second undoped silicon layer 150 lines the hollow interiors corresponding to openings 38b, 39b and 40b.

Referring to Fig. 17, wafer fragment 10b is subjected to processing identical to that discussed above regarding Fig. 10 to convert exposed undoped silicon surfaces to rugged-polysilicon surfaces, while not roughening exposed doped silicon surfaces. Such treatment forms a rugged-polysilicon layer 122b from exposed portions of first undoped silicon layer 146 (shown in Fig. 15) and forms a rugged-polysilicon layer 160 from second undoped silicon layer 150 within the interiors of pedestals 104b, 106b and 108b. Such processing also out-diffuses dopant from doped silicon layer 148 into adjacent undoped layers and thus converts unexposed portions of undoped layer 146 (shown in Fig. 15) into doped regions 119b.

Subsequent processing, similar to the processing discussed above with reference to Figs. 11-13, may be conducted to form a DRAM array from pedestals 104b, 106b and 108b. In such DRAM array, pedestals 104b and 108b would be storage nodes for first and second capacitors, respectively, and pedestal 106b would form a conductive contact to a bitline. Such subsequent processing is not illustrated as the description above regarding Figs. 11-13 is sufficient to enable a person of skill in the art to form a DRAM array from the structure of Fig. 17. It is noted, however, that the storage nodes formed from pedestals 104b and 108b would differ from the storage nodes of Fig. 13 in that the storage nodes formed from pedestals 104b and 108b would have the shape of upwardly open containers, with the interiors of such containers being lined by rugged-polysilicon layer 160.

The above-described DRAMs and capacitors of the present invention can be implemented into monolithic integrated circuitry, including microprocessors.

To aid in interpretation of the claims that follow, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.